

Appl. No. 09/739,897

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)
2. (Previously presented) A method of determining whether a bit disparity in a data stream is acceptable, comprising the steps of:
 - generating an inverted data stream which is a time-synchronous logical inverse of the data stream,
 - simultaneously sampling a data stream and the inverted data stream,
 - detecting a number of samples of the data stream which have a predetermined one of two logical values within a time period,
 - detecting a number of samples of the inverted data stream which have a different predetermined logical value within the same time period,
 - correlating the detected samples of the data stream with the detected samples of the inverted data stream,
 - discarding those samples of the data stream which are detected in which the corresponding samples of the inverted data stream are not also detected;
 - calculating the ratio of the remaining samples in one of the data streams detected to have the corresponding predetermined logical value to the number of samples considered but not discarded, and
 - comparing the calculated ratio with a predetermined acceptable threshold.
3. (Cancelled)
4. (Cancelled)
5. (Currently amended) ~~A bit disparity monitor according to claim 3~~ A bit disparity monitor for monitoring a bit disparity of a data stream comprising:

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a sub-sampler for sub-sampling the data stream;

a detector for identifying a number of samples of the data stream which have a predetermined one of two logical values within a time period;

a counter for counting a number of samples which are being considered within the time period;

a calculator for determining a ratio of the number of samples detected by the detector which have the corresponding predetermined logical value to the number of samples considered; and

a comparator for comparing the ratio with a predetermined acceptable threshold range,

in which the sub-sampler samples at a rate of 50 MHz.

6. (Cancelled)
7. (Cancelled)
8. (Cancelled)
9. (Previously presented) A bit disparity monitor for monitoring a bit disparity of a data stream comprising:

a sub-sampler for sub-sampling the data stream;

a 1's detector coupled to the sub-sampler for identifying those samples of the data stream which have a logical value of one;

a 1's counter coupled to the 1's detector for determining the number of identified samples within a time period;

a samples counter for determining the number of samples within the time period;

a clock generator coupled to the sub-sampler for indicating when a sample should be taken and coupled to the samples counter for indicating when a sample was taken;

a timer coupled to the 1's counter and the samples counter for indicating the start and end of the time period;

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a comparator coupled to the I's counter and the samples counter for comparing the number of identified samples with the total number of samples taken within the time period; and

a memory element coupled to the comparator for storing the comparison results for monitoring.

10. (Previously presented) A bit disparity monitor for monitoring a disparity of a data stream comprising:

an inverter for generating an inverted data stream which is a time-synchronous logical inverse of the data stream;

a sub-sampler for simultaneously sub-sampling the data stream and the inverted data stream;

a first detector for identifying a number of samples of the data stream which have a predetermined one of several logical values within a time period;

a second detector for identifying a number of samples of the inverted data stream which have a different predetermined logical value within the same time period;

a correlator for correlating the samples detected by the first and second detectors and discarding those samples detected by the first detector in which the corresponding sample is not also detected by the second detector;

a calculator for determining a ratio of remaining samples detected by one of the detectors to have the corresponding predetermined logical value to the number of samples considered but not discarded; and

a comparator for comparing the ratio with a predetermined acceptable threshold.

11. (Original) A bit disparity monitor according to claim 10 in which the first detector identifies samples having a value of logical one.

12. (Original) A bit disparity monitor according to claim 10 in which the second detector identifies samples having a value of logical zero.

13. (Previously presented) A bit disparity monitor for monitoring a bit disparity of a data stream comprising:

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an inverter for generating an inverted data stream which is a time-synchronous logical inverse of the data stream;

a first sub-sampler for sub-sampling the data stream;

a second sub-sampler for sub-sampling the inverted data stream;

a 1's detector coupled to the first sub-sampler for identifying those samples of the data stream which have a logical value of one;

a 0's detector coupled to the second sub-sampler for identifying those samples of the inverted data stream which have a logical value of zero;

a samples counter for determining a number of samples within a time period;

a correlator coupled to the 1's detector, the 0's detector and the samples counter for correlating the samples identified by the 0's detector and discarding those samples which are not identified by both the 1's detector and the 0's detector;

a 1's counter coupled to the correlator for determining the number of remaining identified samples within the time period;

a clock generator coupled to the first and second sub-samplers for indicating when a sample should be taken and coupled to the samples counter for indicating when a sample was taken;

a timer coupled to the 1's counter and the samples counter for indicating the start and end of the time period;

a comparator coupled to the 1's counter and the samples counter for comparing the number of identified samples with the total number of samples taken within the time period; and

a memory element coupled to the comparator for storing the comparison results for monitoring.

14. (Cancelled)

15. (Previously presented) A computer-readable medium for storing computer-executable instructions which, when executed by a processor in a bit disparity monitor corresponding to a data stream perform the following steps:

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generating an inverted data stream which is a time-synchronous logical inverse of the data stream,

simultaneously sampling the data stream and the inverted data stream,

detecting a number of samples of the data stream which have a predetermined one of several logical values within a time period,

detecting a number of samples of the inverted data stream which have a different predetermined logical value within the same time period,

correlating the detected samples of the data stream with the detected samples of the inverted data stream,

discarding those samples of the data stream which are detected in which the corresponding samples of the inverted data stream are not also detected;

calculating a ratio of the remaining samples in one of the data streams detected to have the corresponding predetermined logical value to the number of samples considered but not discarded, and

comparing the calculated ratio with a predetermined acceptable threshold.